

REMARKS

As a preliminary matter, Applicant respectfully requests that the Examiner acknowledge receipt of Priority Document No. 11-201667, which was filed in the PTO on July 14, 2000.

Claim Rejections

Claims 1-16 are all the claims pending in the application. Claims 1-16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ishikawa et al. (U.S. Patent No. 5,926,292), hereinafter referred to as Ishikawa.

With respect to independent claims 1 and 10, the Examiner rejects these claims for the reasons set forth on page 2 of the Office Action. With respect to claim 1, Applicant submits that Ishikawa does not teach or suggest all of the features of Applicant's invention, as recited in claim 1. For example, Ishikawa does not teach or suggest the claimed step of "displaying the monochromatic image having a higher gradation resolution by reproducing said image data using the R, G and B cells in said color display device," as recited in claim 1. That is, nowhere does Ishikawa even mention displaying a monochromatic image on a color display device. The Examiner points out that Ishikawa teaches pallet encode circuits (207, 331) that convert an image pixel data into pallet colors. *See Office Action, page 4.* Applicant submits, however, that the pallet encode circuits are only for the purpose of converting an input color image of 24 bits (i.e., 16,777,216 colors) into a 9-bit color image (i.e., 512 colors) in order to display the image on a color display device as a combination of 8-bit R, G, and B data, respectively, and do not involve

displaying a monochromatic image on a color display device. In other words, Ishikawa et al. uses the pallet encode circuits for the purpose of color subtraction. Therefore, any data can be selected if up to 24-bit data is used.

Moreover, Ishikawa is primarily concerned with minimizing the memory capacity necessary for image processing and ensuring that text and image data can be stored together and processed in a simplified manner (*see col. 14, lines 36-49*), but does not teach or suggest that a monochromatic image is displayed on a color display device.

The pallet encoding described by the Examiner has an affect opposite to the present invention. Because Ishikawa relates to memory reduction, Ishikawa converts more image data information to less data information. *See col. 10, lines 1-2*. Ishikawa accepts the reduction of resolution in favor of reduced storage capacity. *See col. 5, lines 39-47*. By contrast, claim 1 describes higher resolution from R, G, B cells. Ishikawa thus teaches away from claim 1.

With respect to independent claim 10, similar the arguments above with respect to claim 1, Applicant submits that Ishikawa does not teach or suggest “a processing unit by which the R, G and B data of the monochromatic image obtained by allotment by said data allotting unit is output to the R, G and B cells for display on said color display device,” as recited in claim 10. The Examiner alleges on page 3 of the Office Action that it would have been obvious to one having skill in the art at the time the invention was made to utilize Ishikawa’s pallet encode circuit and gradation adding circuit to obtain the desired gradation resolution level with respect to R, G and B cells. However, the pallet encode circuit only performs the function described in

the paragraph above and the gradation adding circuit is just for adding pixel data with gradation information and inputting the result to a raster circuit. *See col. 5, lines 8-19.* On the other hand, neither the pallet encode circuit nor the gradation adding circuit involve outputting R, G, and B data of a monochromatic image obtained by allotment by a data allotting unit, for display on a color display device, as described in claim 10.

Also, as indicated above with respect to independent claim 1, Ishikawa et al. uses the pallet encode circuits for the purpose of color subtraction. Therefore, any data can be selected if up to 24-bit data is used.

On the other hand, for example, the data processing unit 16 of the present invention can define the combination of 8-bit R data, 8-bit G data and 8-bit data when converting input monochrome data into R, G and B data, each of which consists of 8 bits and are used for displaying on the color display device.

When displaying an 8-bit monochrome image on a conventional color display device, the combination of R, G and B merely provides 8-bit data based on $R = G = B$. In other words, the gradation of each of R, G and B consists of 256 levels, from which the gradation does not increase in a monochrome display.

On the other hand, the present invention, for example, can use not only data satisfying $R = G = B$, but also data satisfying $R \approx G \approx B$ in the monochrome display on the color display device with a gradation consisting of $(R + G + B)$ levels - to be more specific, when R, G and B each have a gradation of 256 of 768 levels ($R + G + B = 768$). Namely, the present invention is

capable of displaying with a gradation of 768 levels, which are more than the 256 levels each of R, G and B has for the gradation.

Therefore, for at least the above-stated reasons, Applicant respectfully requests that the Examiner withdraw the rejections of independent claims 1 and 10, and indicate that these claims are allowed.

Applicant submits that claims 2-9 and 11-16 are patentable at least by virtue of their dependencies from claims 1 and 10, respectively.

Further, with respect to the rejections of claims 4 and 11, the Examiner merely states that "Ishikawa teaches that when gradations of each of the R, G, and B planes is 256, 24 bits per pixel are required for full display. See col. 1, lines 53-57." *See page 3 of Office Action.* In response, Applicant submits that the Examiner fails to show that Ishikawa discloses each and every respective aspect of claims 4 and 11. Claim 4 recites and claim 11 similarly recites that "a minimum value and a maximum value of said input data respectively correspond to approximate minimum and maximum luminance values as obtained by combining said R, G and B cells." The Examiner's statement does not show and Ishikawa does not even mention a correspondence between minimum and maximum values of input data and minimum and maximum luminance values. Therefore, for at least this reason, Applicant submits that claims 4 and 11 are patentable over the applied reference.

Further, with respect to the rejections of claims 7 and 8, the Examiner only states, "Ishikawa teaches an image area detecting circuit (205) which include (x,y) coordinate values of

the pixel. See col. 11, lines 30-50.” *See Office Action, page 3.* In response, Applicant submits that the Examiner fails to address the specific features of claim 7 and 8. For example, the Examiner fails to even mention and Ishikawa does not teach or suggest “wherein data for each of the R, G and B cells in said input data, if expressed by coordinates (x,y) on a CIE chromaticity diagram, is within a region bounded by coordinates (0.174, 0.0), (0.4, 0.4) and (α , 0.4) (where α is an x-coordinate of a point at which a spectrum locus crosses a straight line that is parallel to an x-axis and which intercepts a y-axis at 0.4),” as recited in claim 7. Further, the Examiner fails to address and Ishikawa does not teach or suggest “wherein said input data and a mass of the data for each of R, G and B cells are used in 1:1 correspondence,” as recited in claim 8. Therefore, for at least these reasons, Applicant respectfully requests that the Examiner withdraw the rejections of claims 7 and 8, and indicate that these claims are allowed.

Further, with respect to claim 9, the Examiner simply states that “Ishikawa teaches pixel data of one frame as well as image processing circuit (204) with respect to timing.” *See Office Action, page 3.* In response, Applicant submits that the Examiner does not mention and Ishikawa does not teach or suggest the specific features of claim 9, including “wherein data for each of said R, G and B cells is allotted to data for a plurality of time-divided frames and the data allotted to each of said time-divided frames is used to perform time-divided driving of said R, G and B cells independently of each other.” Nowhere does Ishikawa disclose this feature.

To further illustrate the distinguishing aspects of the present invention, as recited in claim 9 for example, over Ishikawa, Applicant submits that in the example shown in Table 6 of the present application, the frame data #1, #2, #3 and #4 is displayed in a time-divided manner. To

be more specific, assuming that the least time required for display is represented by “t”, in the pixel of 9-bit data, four pieces of data consisting of 3, 2, 2 and 2 can be sequentially and repeatedly displayed each for the period of time of “t”. Ishikawa, on the other hand, does not teach or suggest such time division display as set forth in the present invention, specifically, as recited in claim 9.

Therefore, for at least the foregoing reasons, Applicant submits that claim 9 is patentable over the applied reference.

Further, with respect to claims 12-16, the Examiner does not even discuss these claims. Applicant submits that these claims are patentable at least because the applied reference does not teach or suggest each and every one of their respective features.

Finally, claims 17-23 are added to round out the scope of protection solicited for the present invention. Claims 17-23 are patentable at least because the prior art does not teach or suggest their respective features.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

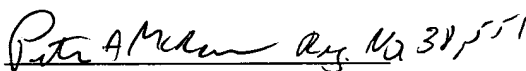
Amendment Under 37 C.F.R. § 1.111
U.S. APPLN. NO. 09/617,308

Applicant hereby petitions for any extension of time which may be required to maintain the pendency of this case, and any required fee, except for the Issue Fee, for such extension is to be charged to Deposit Account No. 19-4880.

Respectfully submitted,

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